HDMI-to-YPbPr Converter

1 Features

YPbPr Output

Up to 1920x1200@60Hz supported
2-channel analog audio supported

HDMI Input

HDMI 1.4a supported
RGB444/YCbCr444/YCbCr422 supported
Pixel clock up to 166MHz
2-channel audio supported
Support Hot-Plug Detect
Adaptive equalization

Clock

Refless clock system

Misc

On-chip 5V to 1.2V regulator
Built-in video test pattern

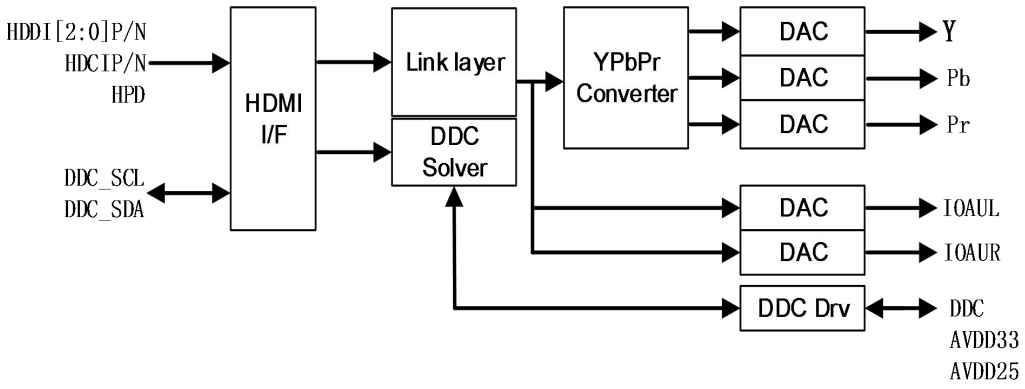
Power

5V or 1.2V core supply
3.3V IO supply
Power consumption ~ **150mA**
Deep-sleep mode power <1mW

Package

QFN-32 (4mm x 4mm) package
RoHS Compliant

2 Block Diagram



3 General Description

NCS8828 is a low-cost, low-power semiconductor device that consists of HDMI receiver,three separate 9-bit video Digital-to-Analog Converters (DACs) and audio encoder, which can convert HDMI signals into YPbPr outputs at a maximum conversion rate of 200MHz with DAC audio output.

The HDMI Receiver integrated is compliant with HDMI 1.4a and support HDCP 1.4 specifications with internal HDCP key.

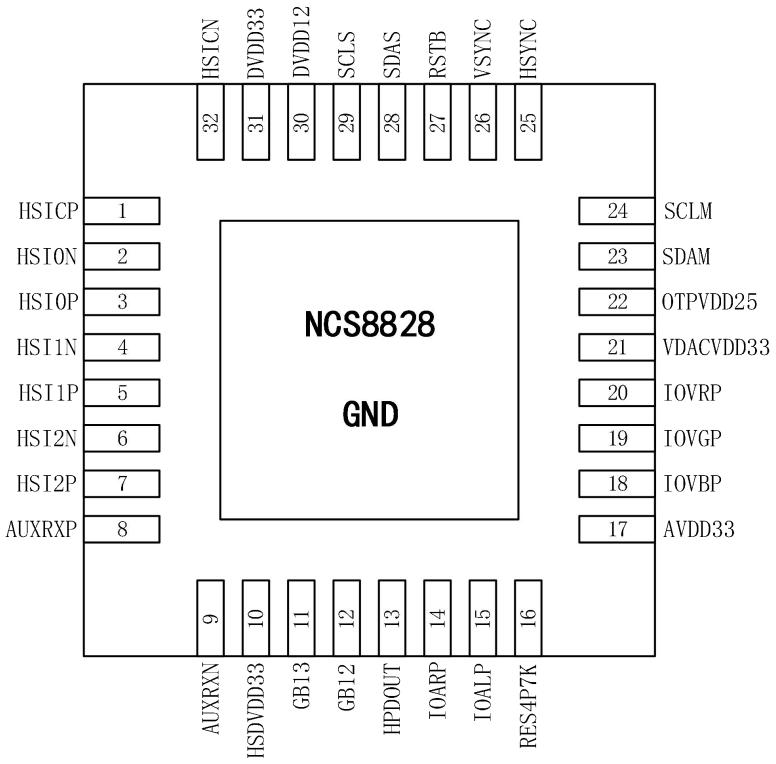
The DACs are based on current source architecture. And the YPbPr output meet VESA VSIS v1r2 clock jitter target. With sophisticated MCU and the Boot ROM embedded,NCS8828 support auto-boot and EDID buffer. Take the advantage of Firmware auto loaded from the

embedded Boot ROM, NCS8828 can support HDMI input detection, DAC connection detection and determine to enter into Power saving mode automatically.

NCS8828 is typically required to support WUXGA (1920x1200) and above at 60Hz frame rate and Minimum support to XGA (1024*768@60Hz) fail safe mode.

Thanks to our proprietary scaling algorithm, NCS8828 provides high picture quality. All the functions pack into a small 4mm*4mmQFN32 package which saves the precious space in mobile devices.

4 Pin Diagram



(Top view)

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5 Pin Description

No.	Pin Name	Description
1	HSICP	HDMI clock channel positive
2	HSION	HDMI data channel 0 negative
3	HSIOP	HDMI data channel 0 positive

4	HSI1N	HDMI data channel 1 negative
5	HSI1P	HDMI data channel 1 positive
6	HSI2N	HDMI data channel 2 negative
7	HSI2P	HDMI data channel 2 positive
8	AUXRXP	AUX channel positive
9	AUXRXN	AUX channel negative
10	HSDVDD33	3.3V power supply for HDMI
11	GB13	GPIO13
12	GB12	GPIO12
13	HPDOUT	Hot-Plug Detect output
14	IOARP	DAC_R Output
15	IOALP	DAC_L Output
16	RES4P7K	Rvref
17	AVDD33	3.3V power supply for ***
18	IOVBP	VGA Blue Output
19	IOVGP	VGA Green Output
20	IOVRP	VGA Red Output
21	VDACVDD33	3.3V power supply for VGA
22	OTPVDD25	2.5V power supply for ***
23	SDAM	Master I2C data
24	SCLM	Master I2C clock
25	HSYNC	Horizontal synchronization
26	VSYNC	Vertical synchronization
27	RSTB	Reset, active low
28	SDAS	Slave I2C data
29	SCLS	Slave I2C clock
30	DVDD12	1.2V power supply for digital
31	DVDD33	3.3V power supply for digital
32	HSICN	HDMI clock channel negative
Thermal	GND	Ground

6 Electrical Specifications

6.1 Operating Conditions

Symbol	Description	Min	Typ	Max	Units
HSDVDD33	3.3V power supply for HDMI	3.14	3.3	3.46	V
AVDD33	3.3V power supply for analog	3.14	3.3	3.46	V
VDACVDD33	3.3V power supply for VGA	3.14	3.3	3.46	V

DVDD33	3.3V power supply for digital	3.14	3.3	3.46	V
OTPVDD25	2.5V power **supply for analog**	2.37	2.5	2.62	V
DVDD12	1.2V power **supply for digital core**	1.14	1.2	1.26	V
Temp	Ambient temperature	-20	25	85	℃
ESD	HBM				kV
	CDM				V
	MM				V

6.2 Power Consumption

Mode	Power				
	HSDVDD33	AVDD33	VDACVDD33	DVDD33	Power
1080I @ 60Hz					
1080P @ 60Hz					
720I @ 60Hz					
720P @ 60Hz					
576I @ 60Hz					
576P @ 60Hz					
Deep-sleep	-				

Note:

1.

2.

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6.4 HDMI Electrical Specification

Symbol	Description	Min	Typ	Max	Units
$Rate_{HDMI}$	HDMI data rate per pair			3000	Mbps
$f_{CLK-HDMI}$	HDMI input TMDS clock frequency			320	MHz
$V_{TH-HDMI}$	Differential input high threshold			0.1	V
$V_{TL-HDMI}$	Differential input low threshold	-0.1			V
C_{RX}	AC coupling capacitor	75	100	200	nF
T_{jitter}	HDMI input TMDS clock jitter			0.3	T_{bit}
$T_{skew-intra-pair}$	Skew between differential pair,TMDS clock below 222.75MHz			0.4	T_{bit}
$T_{skew-intra-pair}$	Skew between differential pair,TMDS clock above 222.75MHz			$0.15T_{bit}$ + 112ps	-
$T_{skew-inter-pair}$	Skew between differential channel			$0.2T_{character}$+ 1.78ns	-

7 Register Table

8 Applications

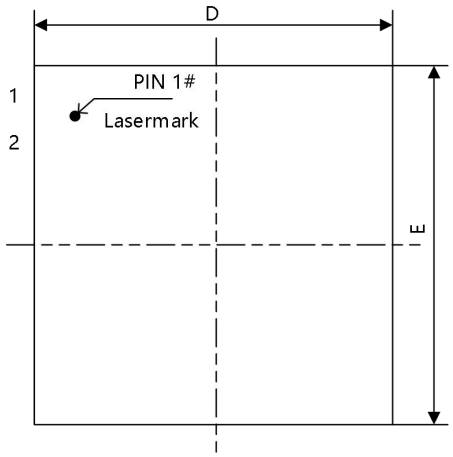
8.1 Typical Application Schematics

8.2 PCB Layout Rules

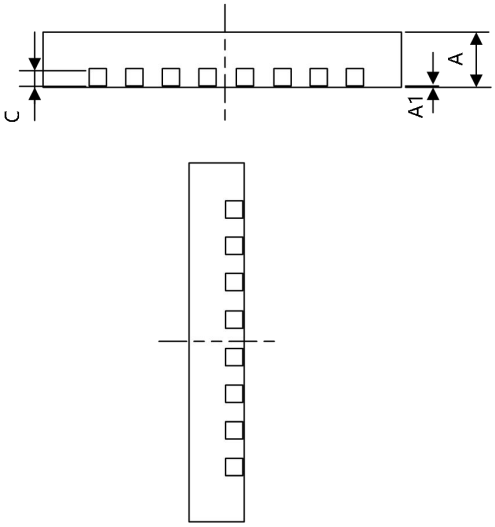
a. HDMI inter-lane skew is suggested to be controlled under 50mil.

8.3 Power-on Sequence

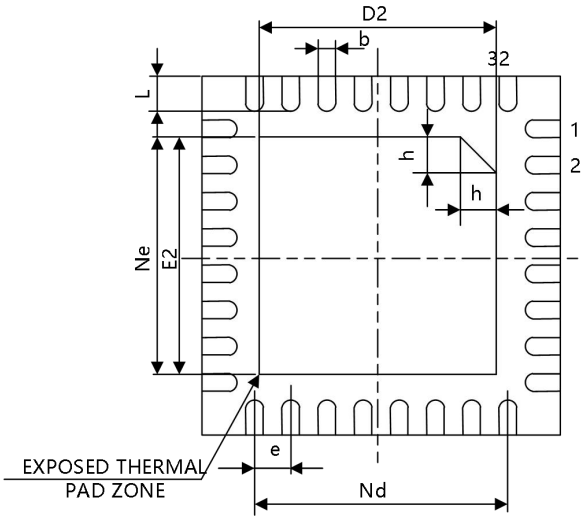
9 Package



TOP VIEW



SIDE VIEW



BOTTOM VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e	0.40BSC		
Ne	2.80BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40
L/F载体尺寸	122*122		

10 Revision History

Rev. #	Date	Author	Comments
0.92	12/15/2016	Xin Zhang	First beta release

This document contains information on a new product. Specifications and information herein are subject to change without notice.